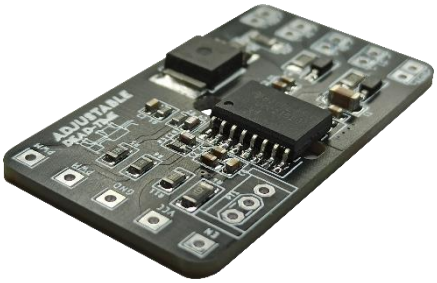
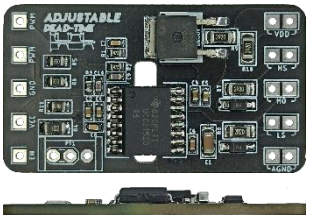
ISOLATED GATE DRIVER

DI4A-05W21A





FEATURES

- Programmable Dead-Time: 5 ns – 5 µs
- Configurable Outputs:
  - Two Low-Side Driver
  - Half-Bridge (High&Low Side) Driver
- Reinforced Isolation:
  - Common-Mode Transient Immunity: >100V/ns
  - ESD Protection: 12.8 kV
- High Peak Current:
  - Peak Source: 4A
  - Peak Sink: 6A
- Noise Filtering: <5 ns
- Under Voltage Lock-Out (UVLO) Protection: 8V
- High Frequency Switching: 5 MHz

APPLICATIONS

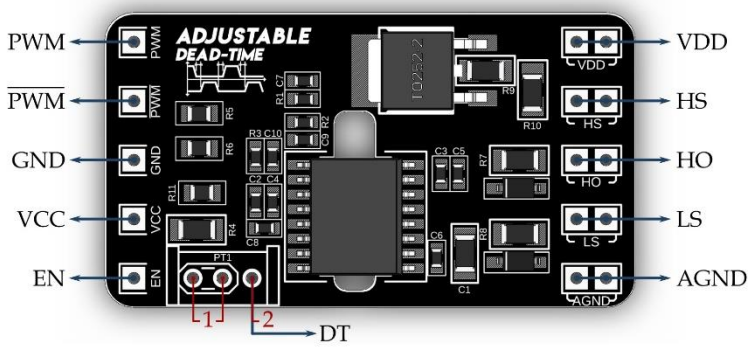
- Battery Chargers.
- Isolated Converters in DC-DC and AC-DC Power Supplies.
- Server, Telecom and Industrial Infrastructures.
- Motor Driver and LED Lighting.
- DC-to-AC Solar Inverters.
- Inductive Heating.
- UPS (Uninterruptible Power Supply).

GENERAL DESCRIPTION

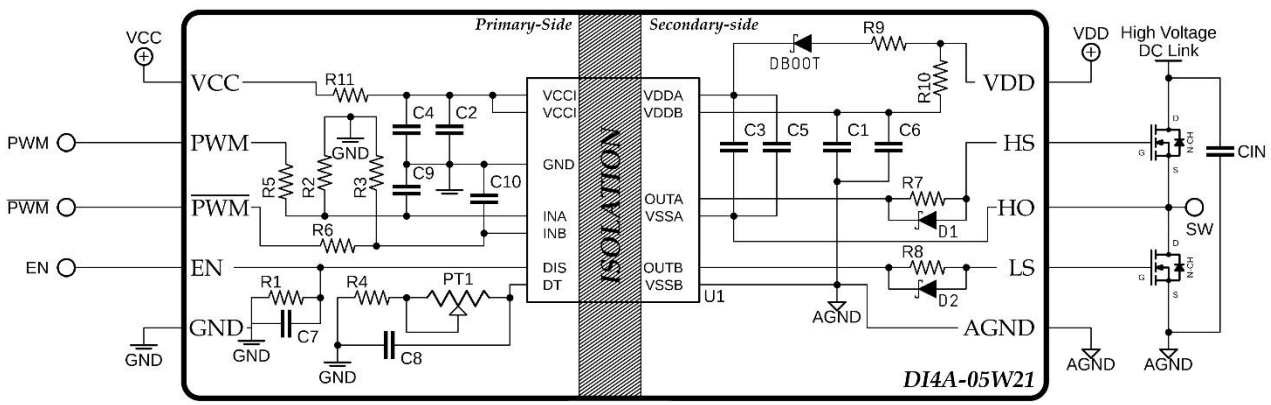
DI4A-05W21A is a two-channel isolated Gate driver module with 4A peak source and 6A peak sink current. The module stands out with its programmable Dead-Time feature, its outputs can be configured as two low-side drives and half-bridge drives.

UCC21520 IC used on the module is designed to drive power MOSFETs, IGBTs, and SiC MOSFETs up to 5-MHz with best-in-class propagation delay (Max. 30 ns) and pulse-width distortion (Max. 5 ns). Input and output are isolated from each other with 100V/ns common-mode instantaneous protection capability (CMTI) and 5.7kVrms isolation capability in UL 1577 standards.

DESCRIPTION WITH IMAGE



PIN CONFIGURATION



PT1 – TRIMMERPOT 500K | R1, R2, R3 - 4.7K Ohms 5% 1/10W 100PPM | R4 - 1K Ohms 5% 1/4W 100PPM 1206 (3212 Metric) | R5, R6 - 33 Ohms 5% 1/8W 200PPM | R7, R8, R9, R10 - 2.2 Ohms 1% 1/4W 400PPM | R11 - 1 Ohms 1% 1/8W 400PPM | D1, D2 - MBR0540-HT | DBOOT -C3D02060E | U1 - UCC21520DWR | C1 - 10uF 50VDC ±10% X5R | C2, C3 - 1uF 50VDC ±10% X5R | C4, C5, C6 - 220nF 50VDC ±10% X7R | C7, C8 - 1nF 50VDC ±10% X7R | C9, C10 - 10pF 50VDC ±5% C0G

Pin		*Descriptions*	*Notes*
INPUTS	PWM	Signal Input 1	TTL/CMOS compatible input threshold.
	$\overline{PWM}$	Signal Input 2	Tie this pin to ground if not used.
	GND	Primary-Side Ground Reference.	All signals in the primary side are referenced to this ground.
	VCC	Primary-Side Supply Voltage.	Suggested 3V-18V.
	EN	Enable Pin. (1: Disable – 0: Enable)	Disables both driver outputs if asserted high, enables if set low or left open.
	DT	Dead-Time Programming Input.	It can be programmed with the resistance to be placed between 1 and 2. For details see. ***Programmable Dead-Time..***
OUTPUTS	VDD	Secondary-Side Supply Voltage.	Suggested 9-25V
	HS	High-Side Signal Output.	–
	HO	High-Side Offset Point.	The ground reference of the HS Output.
	LS	Low-Side Signal Output.	–
	$AGND$	Secondary-Side Ground Reference.	The ground reference of the LS Output.

Table 1: *Pin Configurations.*

Note: Internal pull-down is available at PWM, $\overline{PWM}$, EN ve DT inputs. If these inputs will not be used, they can be left without any connection. However, it is recommended to make GND connection of unused inputs for best noise protection.

Programmable Dead-Time and Overlap

Variable Dead-Time: You can use the variable Dead-Time feature when you solder the 500K trimmer that comes with DI4A-05W21A to the place named PT1 on the PCB. (**Figure 1(A)**)

$$R_{DT} = R4 + PT1 \quad (1)$$

$$t_{DT}[ns] = 10 * R_{DT}[K\Omega] \quad (2)$$

Dead-Time is calculated according to the formula (2). Note: ($R4 = 1\ K\Omega$)

Fixed Dead-Time: If a fixed value is suitable for you, you can use a fixed resistance in the place called PT1 (**Figure 1(B1)**) or you can change the R4 resistance directly by shorting the PT1 ports. (**Figure 1(B2)**)

Note: Package/Case information for R4: 1206 (3212 Metric)

Overlap: By connecting the DT pin to the VCC, you can turn off the "Dead-Time" feature and allow the overlaps (The event that the voltage levels at the outputs are at the high logic level at the same time). (**Figure 1(C)**)

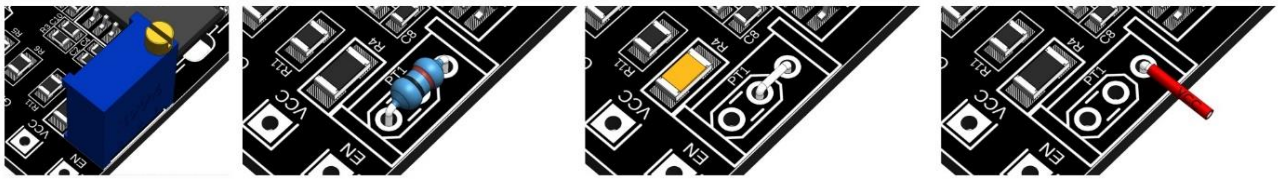


Figure 1: ***(A)*** *Using trimmer for variable Dead-Time,* ***(B1)*** *Using 1/8W resistor for fixed Dead-Time,* ***(B2)*** *Replacing R4 for Fixed Dead-Time (Package/Case: 1206 (3216 Metric)) and shorts the PT1 connection.*
(C) *Applying VCC voltage to DT pin to allow overlaps.*

Logic Relationship of Inputs and Outputs

Inputs		*Enable Pin*	*Outputs*		*Notes*
$PWM\ (ENA)$	$\overline{PWM}\ (ENB)$		$HS\ (OUTA)$	$LS\ (OUTB)$	
L	L	L	L	L	If Dead Time function is used, output transitions occur after the dead time expires.
L	H	L	L	H	
H	L	L	H	L	
H	H	L	L	L	DT is left open or programmed with R_{DT}
H	H	L	H	H	DT pin pulled to VCC
NC	NC	L	L	L	–
X	X	H	L	L	–

Table 2: *Input/output Logic Table.*
L: Low, **H:** High, **NC:** No Connection, **X:** Any Value

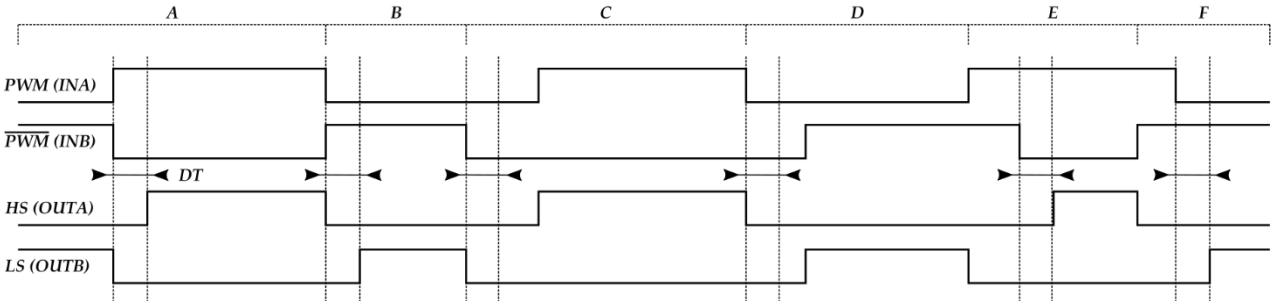


Figure 2: *Input/output Logic Relationship For A, B, C, D, E and F Conditions.*

Using the Module as a Half-Bridge Driver and Low-Side Driver Only

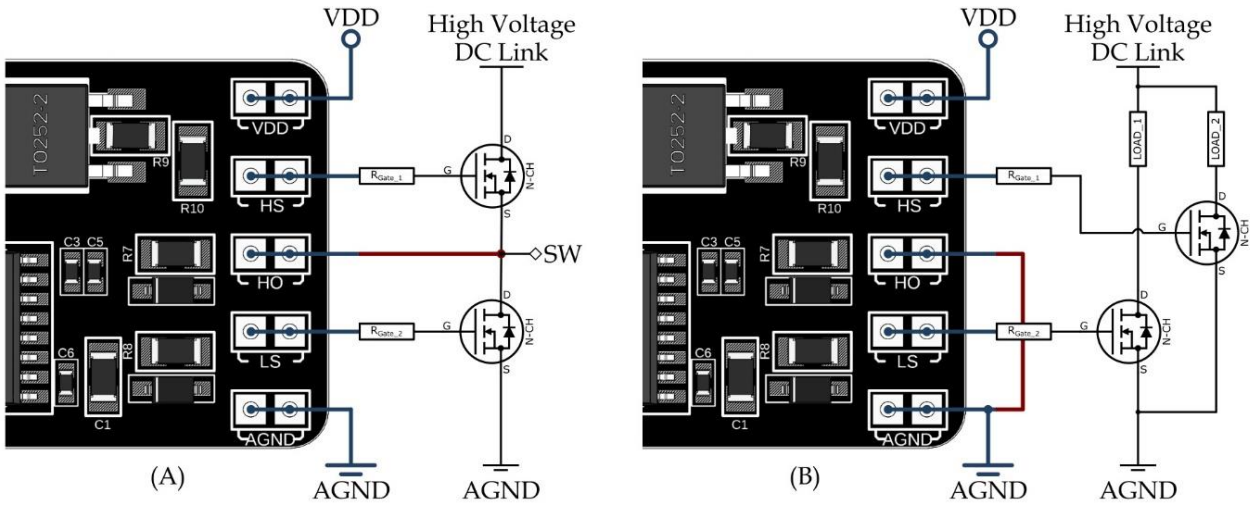


Figure 3: ***(A)*** *Using the Module as a Half-Bridge Driver,* ***(B)*** *Using the Module as a Low-Side Driver Only.*

ELECTRICAL SPECIFICATIONS

Pushing the device to operate above the "Max." listed in the table below may cause the device to overheat and to take up permanent damage. It is inconclusive that the device will function beyond the operating limits as set out in this technical document. Prolonged exposure to work under "maximum" rating conditions may affect device reliability.

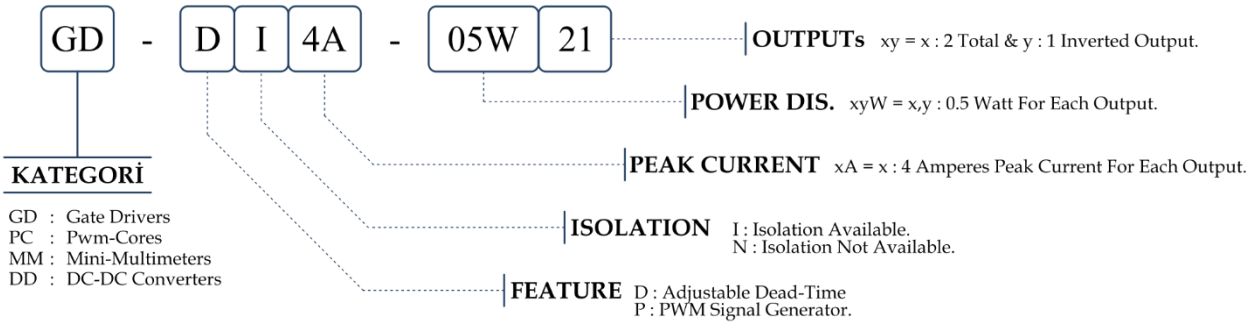
Table 3: *Electrical Specifications.*

Conditions: Unless Otherwise Noted, $T_O = +25^oC$ ve $3.3V \leq V_{CC} \leq 5V$ ve $V_{DD} = 12V$ ve C_L = 100 pF ve R_7 & $R_8 = 0\Omega$.							
Parameters		**Sym**	**Min**	**Typ**	**Max**	**Units**	**Condition**
Input							
Primary-Side Input Voltage		V_{CC}	3	–	18	V	DC
Secondary-Side Input Volt.		V_{DD}	9	–	25	V	
Threshold Voltage, High		V_{PWMH}, V_{ENH}	1.6	1.8	2	V	
Threshold Voltage, Low		V_{PWML}, V_{ENL}	0.8	1	1.2	V	
Threshold Hysteresis		$V_{PWM_{HYS}}$ V_{EN_HYS}	–	0.8	–	V	
Output							
Output Voltage, High&Low		$V_{H(HS,LS)}$	0.055	–	V_{DD} – 0.05	V	$V_{DD} = 12V$
Output Resistance, High		$R_{OUT,HIGH}$	–	5	–	Ω	
Output Resistance, Low		$R_{OUT,LOW}$	–	0.55	–	Ω	
Peak Output Current*	Source	$I_{HS+,LS+}$	–	–	4	A	
	Sink	$I_{HS-,LS-}$	–	–	6	A	
Switching							
Rise Time (From 20% to 80%)		t_R	–	6	16	ns	C_L = 1.8 nF
Fall Time (From 90% to 10%)		t_F	–	7	12	ns	C_L = 1.8 nF
Propagation Delay		t_{PD}	14	19	30	ns	
Pulse Width Distortion		t_{PWD}	–	–	5	ns	
Output Power Dissipation		W_{PD}	–	–	1.00	W	**Note 1**

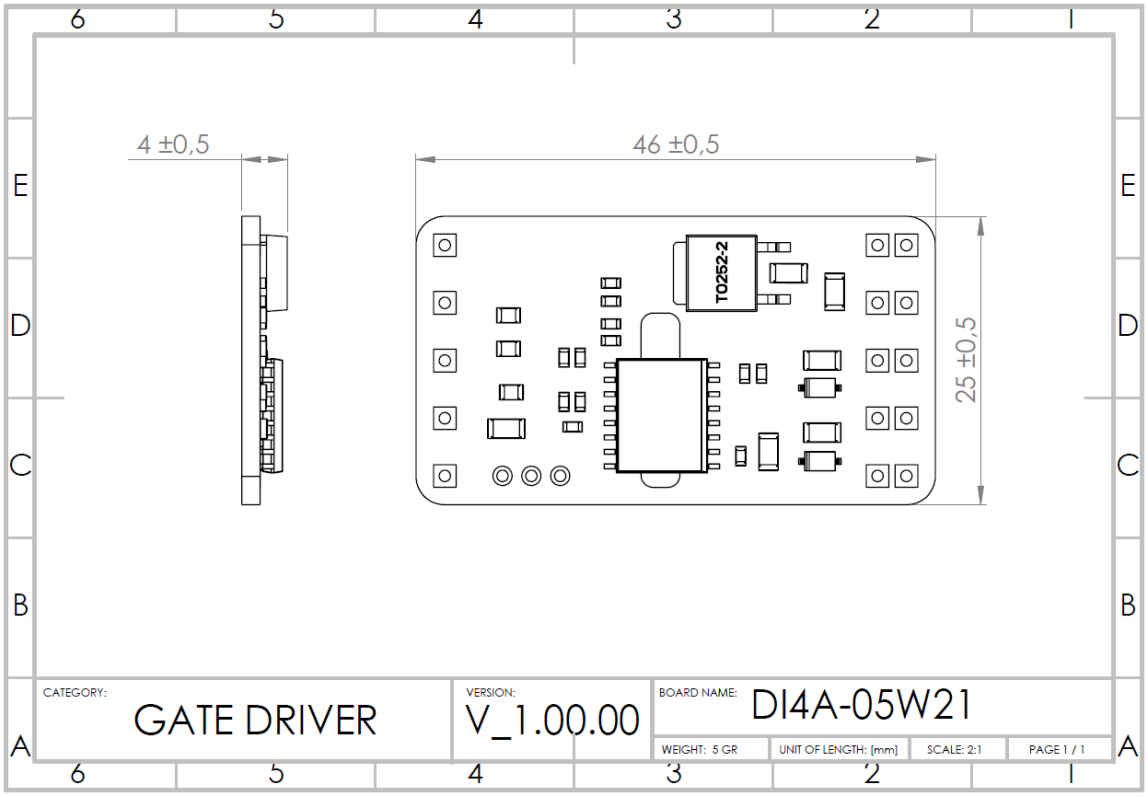
* **:** It refers to the peak current value that can be provided from each of the signal outputs.

Note1 **:** It refers to the power that can be consumed in the total of the signal outputs.

PRODUCT CODE



TECHNICAL DRAWING



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